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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,673	01/07/2004	I-Sheng Liu	M-15281 US	6785

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EXAMINER	
MONDT, JOHANNES P	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 02/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/753,673	LIU ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE ____ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12/14/04 (prel. Am.) and 1/20/05 (Resp)*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *10-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1-9 in the reply filed on January 20, 2005 is acknowledged.

Drawings

2. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the Drawings thus far submitted are informal. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Specification

The Preliminary Amendment to the Specification has been approved by the examiner.

Information Disclosure Statement

The examiner has considered the item listed on the Information Disclosure (IDS). A signed copy of FORM PTO/SB/08A is enclosed with this office action.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. ***Claims 1-3*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,912,842) in view of Kang et al (6,180,443 B1). *Chang et al teach* a two-transistor PMOS memory cell (see title and abstract, first sentence), comprising: a PMOS select transistor 40b (col. 4, l. 2 and Figure 3) having a drain and source 50 and 48, respectively (cf. col. 4, l. 3-7), formed as separate P+ diffusion regions in an N- well 42 (col. 4, l. 2); a PMOS floating gate transistor 40a (cf. col. 4, l. 1) having a drain and a source 46 and 48 (cf. col. 4, l. 6-9) formed as separate P+ diffusion regions in the N-well, wherein the P+ diffusion region 48 that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source (col. 4, l. 4-6).

Chang et al do not necessarily teach an N implant underlying the P+ diffusion region that forms the floating gate transistor's drain.

However, it would have been obvious to teach an N implant underlying the P+ diffusion region that forms the floating gate transistor's drain in view of Kang et al, who, in a patent on a method to achieve improved performance of a semiconductor device with two MOS transistors of the same conductivity type with common source/drain diffusion region (title, abstract and col. 1, l. 18 – col. 2, l. 12 and col. 3, l. 31- col. 4, l. 30), including in particular prevention of punch-through (col. 3, l. 31 -col. 4, l. 30), - hence closely related to the invention by Chang et al, teach the inclusion of halo implants 30 (col. 5, l. 13-15) underlying the common source/drain diffusion region and of a conductivity type opposite to that of said common source/drain diffusion region. While

combination of the teaching in this regard by Kang et al meets the claim limitation considering the p-type conductivity of the P+ diffusion regions as claimed, resulting in an N implant underlying said common source/drain region, *motivation* for inclusion of the teaching by Kang et al in this regard in the invention by Chang et al derives from the resulting additional protection against punch through.

On claim 2: in the combined invention the lateral extent of the M implant 30 is substantially the same as that of the P+ diffusion region that forms the PMOS floating gate transistor's drain, i.e., region 48, because the tilt angle of the halo implant can be zero degrees (col. 6, l. 33-41)

On claim 3: the drain of the PMOS select transistor 50 couples to a bit line BL0 of a memory array 70 (cf. col. 5, l. 1-15), and a select gate 40 b of the PMOS select transistor couples to a word line WL0 (loc.cit.) of the memory array 70.

On claim 6: the memory cell is configured such that the floating gate transistor may be programmed using band-to-band tunneling because a thin tunnel oxide layer 56 (col. 31-33) is included while the two transistors are PMOS transistors.

On claim 7: Fowler-Nordheim tunneling is implemented in a preferred embodiment in Chang et al (col. 5, l. 63 – col. 7, l. 51).

5. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Kang et al as applied to claim 2 above, and further in view of Cang et al (5,687,118). In the combined invention by Chang et al and Kang et al a floating gate 54 is formed in a first polysilicon layer (col. 4, l. 8-9). Neither Chang et al nor Kang et al necessarily teach the control gate of the PMOS floating gate transistor to be formed of

polysilicon. However, it would have been obvious to include the further limitation on the material constitution of said control gate as claimed in view of Chang et al (5,687,118) ("Chang 2" henceforth) who teach in very closely related art the material constitution of the control gate to be polysilicon as well (cf. col. 11, l. 46-56). Motivation to include the teaching by Chang2 at least stems from the economy to use the same material for extremely similar structures in the same invention. Furthermore, Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. *In re Leshin* 125 USPQ 416. Chang2 proves that polysilicon for the material selection of the control gate in a floating gate transistor is generally understood to be suitable.

6. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Kang et al as applied to claim 2 above, and further in view of Yaegashi et al (US 2002/0098638 A1). As detailed above, claim 2 is unpatentable over Chang et al in view of Kang et al *Although Chang et al teach* the memory cell to include a single plysilicon layer containing a floating gate (col. 4, l. 9-11 and Figure 3, *neither Chang nor Kang necessarily teach* the further limitation as defined by claim 5. *However, it would have been obvious* to include said further limitation in view of Yaegashi et al who teaches a back-gate as control gate to facilitate erase operations (see paragraph [0347] and Fig. 71). *Motivation* to include the teaching by Yaegashi et al in the invention thus derives at least from facilitating an operation that is routinely performed by any memory cell including that of the invention.

7. ***Claims 8-9*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Kang et al as applied to claim 2 above, and further in view of Prall et al (5,345,104). As detailed above, claim 2 is unpatentable over Chang et al in view of Kang et al. Neither necessarily teach the further limitations of either claim 8 or claim 9. *However, it would have been obvious to include the further limitation as defined by claim 8 in view of Prall et al*, who, in a patent on creating halo regions in a MOSFET with floating gate within the context of a flash memory cell, - hence closely related art, teach the thickness of the drain region 18 of the floating gate's transistor to be approximately 1000 Angstrom = 0.1 micron (cf. col. 3, l. 55-60), which is in the range as claimed in claim 8, considering the verbiage "approximately". Furthermore, the halo implantation step by Kang et al produces a depth of about 0.3 microns, considering phosphorus ions are implanted at an energy of about 100 keV, which implies a thickness of the N implant of about 0.3-0.1 = 0.2 microns, meeting the limitation of claim 9. Applicant is reminded that a *prima facie* case of obviousness typically exists when the ranges of a claimed quantity overlap the ranges disclosed in the prior art or when the ranges of a claimed quantity do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
February 22, 2005

Patent Examiner:

Johannes Mondt (Art Unit: 2826)